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Folded Cascode Operational Amplifier Design Utilizing 0.25 µm CMOS Technology

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ABSTRACT: A one-stage Folded Cascode Operational Amplifier with the self-biasing scheme for the PMOS differential input stage is designed by using LTspice simulator and the designing procedure is described. This folded op amp will have a high Common-mode input range (ICMR) and a high maximum voltage output thereby high gain. The LTspice simulation results correlate very well with the hand calculations obtained theoretical values. All the MOSFETs are kept in saturation to ensure high open loop gain. Then, a two-stage op amp circuit has been designed by assuming Zero (z)= 10 GB, and phase margin (PM= 68o). The obtained result of the output gain for this design was Avo= 91 dB, indicating that the design has a high gain.

Keywords: High ICMR, high open loop DC voltage gain, power dissipation, Zero (z), phase margin (PM)

1. INTRODUCTION

Complementary Metal Oxide Semiconductor (CMOS) technology is constantly scaled down to realize low-cost, high-speed, high-density, and low-power digital systems. Because of the rapid evolution in digital CMOS technology, single-chip solutions becoming a charming process for systems when the elaboration is increased [1]. The development of integrated circuit (IC) technologies for three conventions in the past, the world has been faced rapid growth to cope up with forever always growing elaborations of signal processing systems [2-4]. Several applications can be utilized with the ICs such as radar, medical imagining technique, speech processing, satellite communication, instrumentation, sonar, and communications, … etc [5, 6]. One of the most core parts of the several mixed analog and signal circuit design system is the Operational amplifier (Op-amps) [7, 8]. In general, op-amps are classified into many kinds of topologies for example two-stage op-amp folded cascode op-amp and telescopic op-amp [9, 10]. A PMOS differential folded cascode op-amps circuit has been designed in this paper. The LTspice software is used for the designing and simulation [11-23].

2. MATERIALS AND MOTHOD

This study is divided into two milestones; the first milestone shows the one-stage folded op-amp, while in the second milestone two-stage is implemented. The software used to design both milestones is LTspice.

Milestone 1

The main goal in this milestone is to design a one-stage folded op amp with self-biasing scheme to the following specifications:

- Power dissipation ≤ 2.5 mW
- Open loop DC voltage gain, |Av0| ≥ 500
- Overdrive voltage, |VOD| = 0.3 V for all transistors excluding the input pair
- Gate length, L = 2 µm for all transistors

The design of the circuit obtained for required folded op amp as shown in Figure 1

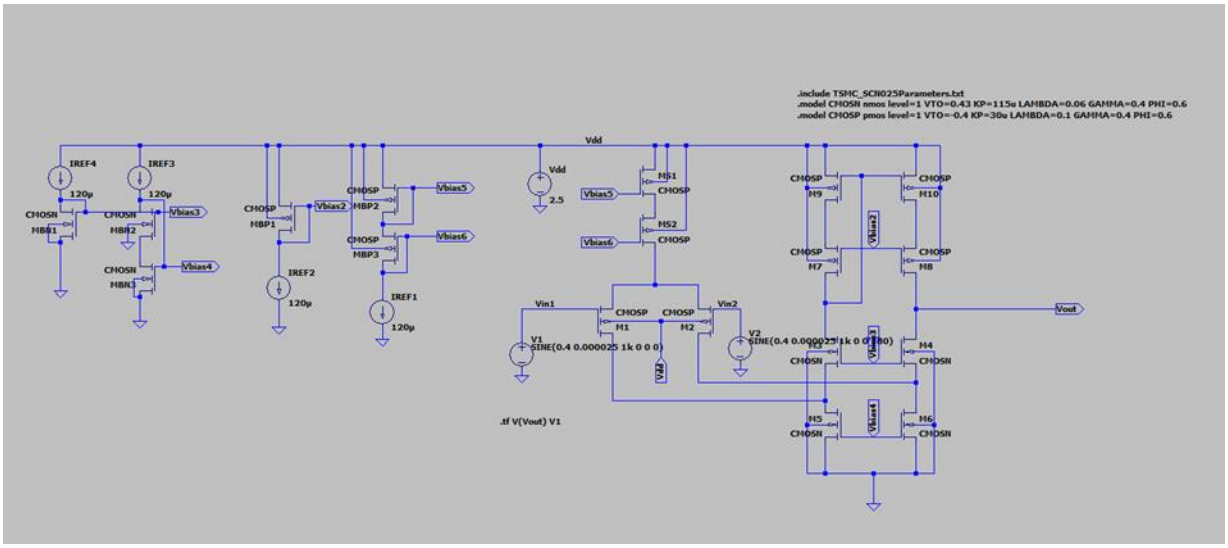

FIGURE 1. - One-stage folded cascode operational amplifier

In Figure 1, I_{ref} and I_{ss} assumed to be 120 µA. The circuit designed in such a way that all the MOSFETs are in saturation which can be seen in obtained hand calculations. The widths obtained for the biasing circuit, some changes are done so that all the transistors may come in saturation. As width of MBN1 has been changed to 8.8 µm from the hand calculated value 11.59 µm. And width of MBP1 is reduced to (32 from 44.44) µm (hand calculated value). To get 0.52 V overdrive for both M_1 and M_2, its widths have been changed to 30 µm.

The widths and biasing of the circuit in Figure 1 have been calculated using the values considered for power dissipation and open loop DC voltage gain (given in the specifications).

3. DESIGN PROCEDURE

In milestone 1, for the given specifications, a one-stage folded cascode Operational Amplifier is designed with the self-biasing scheme for the PMOS differential input stage. The design procedures are as follows:

- At first, the different components of the op amp are named like the transistors, biasing circuit and input voltages.
- Tail current replicated with the help of a cascode current source and implemented all the bias voltages for the op amp with the high-swing cascode current mirror biasing circuit (improved). Details of the procedure can be seen from the circuit diagram in Figure 1 and the hand-calculations as shown in Table 1.

Table 1. – Op-amp Parameters

Parameter	Value
$\|I_{SS}\|$	120 µA
$\|I_{D5}\|$	120 µA
$\|I_{D6}\|$	120 µA
$\|V_{OD1}\|$, $\|V_{OD2}\|$	0.52 V
$V_{ICM(min)} < ICMR < V_{ICM(max)}$	-0.1<ICMR<0.98
$V_{O(max)} < V_O < V_{O(max)}$	0.66< V_o <1.82

Now, determining Input Common-Mode Range (ICMR) by obtaining the transfer curve plot using DC analysis. Then, choosing a particular value of VIN, CM such that current source is operating and transistors M_1 and M_2 are in saturation. Then, running the operating point analysis (.op) to verify the correct operation of the circuit. Thus, from it's result, ensuring that M1 ~ M10 transistors are saturated by changing the width values if needed as shown in Table 2.

Table 2. - Saturated values of transistors $M_1 \sim M_{10}$

	M_1, M_2	M_3, M_4	M_5, M_6	M_7, M_8	M_9, M_{10}
V_{dsat} (V_{OD})	0.68	0.3	0.3	0.3	0.3
V_{ds}	1.18	1.5	0.308	0.39	0.306
Saturated ?	Yes	Yes	Yes	Yes	Yes

Finally, measuring the gain using the transient analysis (.tran), the frequency of the small-signal is set as 1 kHz and its amplitude as 0.025 mV for both V_{in1} and V_{in2}. But, the V_{in2} is having 180° phase difference with respect to V_{in1} to bring the circuit in Differential mode, and then measuring the differential gain by measuring the peak-to-peak output signal divided by the differential input signal, also running transfer function analysis (.tf) to confirm the gain as shown in Table 3.

Table 3. - The values of power dissipation and output gain

Parameter	Value
P_D	1.8 mW
A_{VO}	1646

4. RESULTS AND DISCUSSION

4.1 RESULT OF THE OPERATING ANALYSIS: NETLIST FILE OF THE DESIGN

Figure 2 shows the value of V_{out} of the designed circuit.

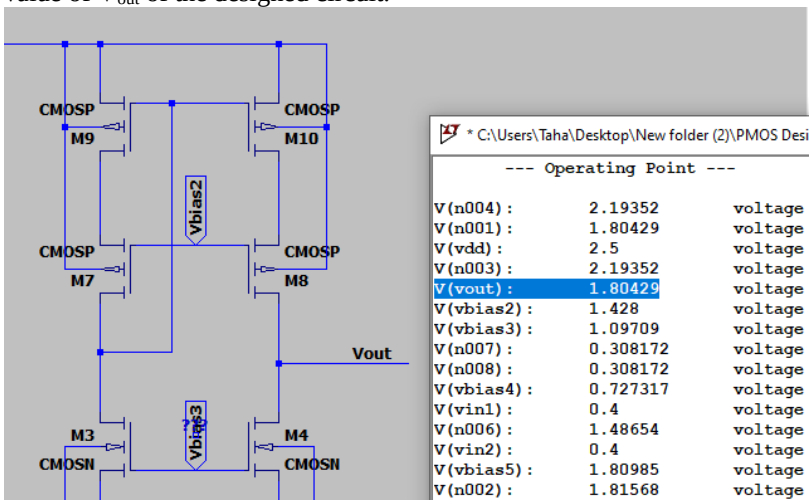

FIGURE 2. - Output voltage of the designed circuit

From the above operating points, the correct operation of the circuit is verified. The values of the different nodes of the circuit ensure that all the transistors are in saturation. Moreover, all the results obtained are matched by hand calculations.

W/L Ration of the Transistor

$$\frac{W}{L} = \frac{I_{SS}}{\frac{1}{2}\mu C_{ox} V_{DSAT}} \quad (1)$$

→ PMOS transistor

$$\frac{W}{L} = \frac{I_{SS}}{K_P V_{DSAT}} \quad (2)$$

$$Gain = g_{m1}([g_{m7}.r_{ds7}.(r_{ds1} \backslash\backslash r_{ds9})] \ \backslash\backslash \ [g_{m3}.r_{ds3}.r_{ds5})]) \quad (3)$$

4.2 TRANSFER CURVE PLOT

Figure 3 shows the transfer curve plot of the designed circuit.

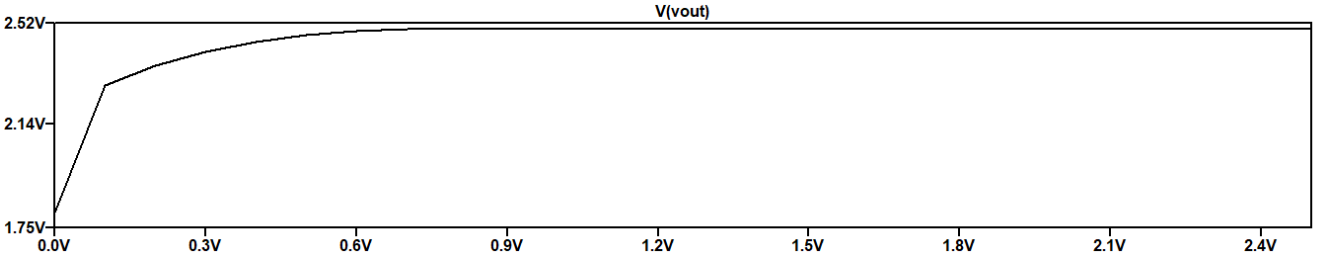

FIGURE 3. - Transfer curve plot

By using the DC analysis, the transfer curve plot is obtained as in figure 3. sweeping the voltage of V_{in1} from (0 to 2.5) V with step of 0.1 V to see the ICMR range of the design for which the circuit is working correctly. Thus, 0.4 V is chosen as the common mode voltage for the proper Dc operation. The maximum output voltage from the plot in Figure 3 is gotten, of about 2.496 V.

4.3 TRANSIENT PLOTS

Figure 4 shows the transient plot of the designed circuit.

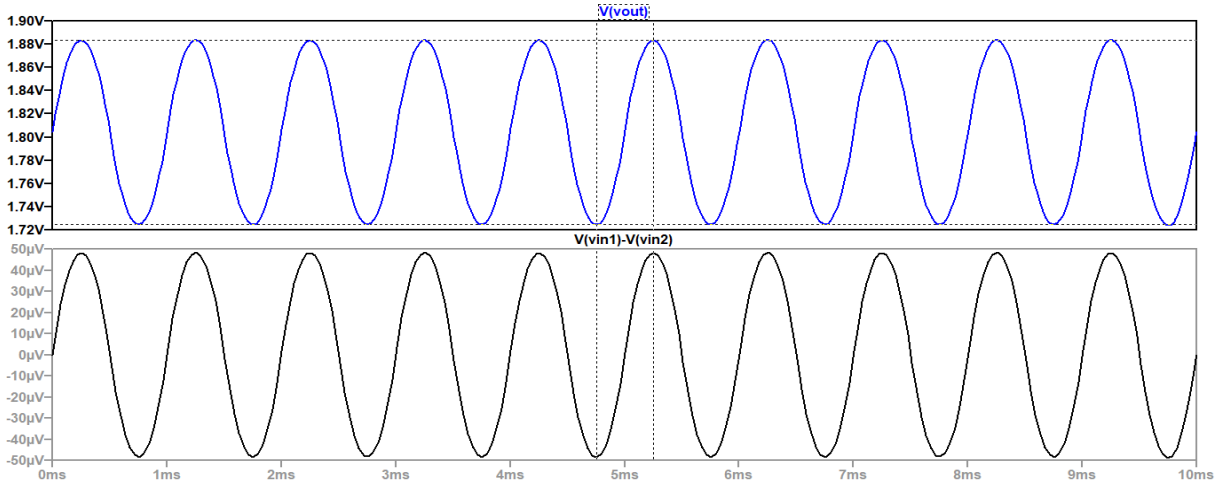

FIGURE 4. - Transient plot of the designed circuit

For transient plot in Figure 4, the frequency of the small-signal is set as 1 kHz and its amplitude as 0.025 mV for both V_{in1} and V_{in2}. But, the V_{in2} is having 180 degree phase difference with respect to V_{in1} to bring the circuit in Differential mode, and then measuring the differential gain by measuring the peak-to-peak output signal divided by the differential input signal. The open loop DC voltage gain is got as 1646 for the above design.

4.4 TRANSFER FUNCTION OUTPUT

Figure 5 shows the transfer function output of the designed circuit.

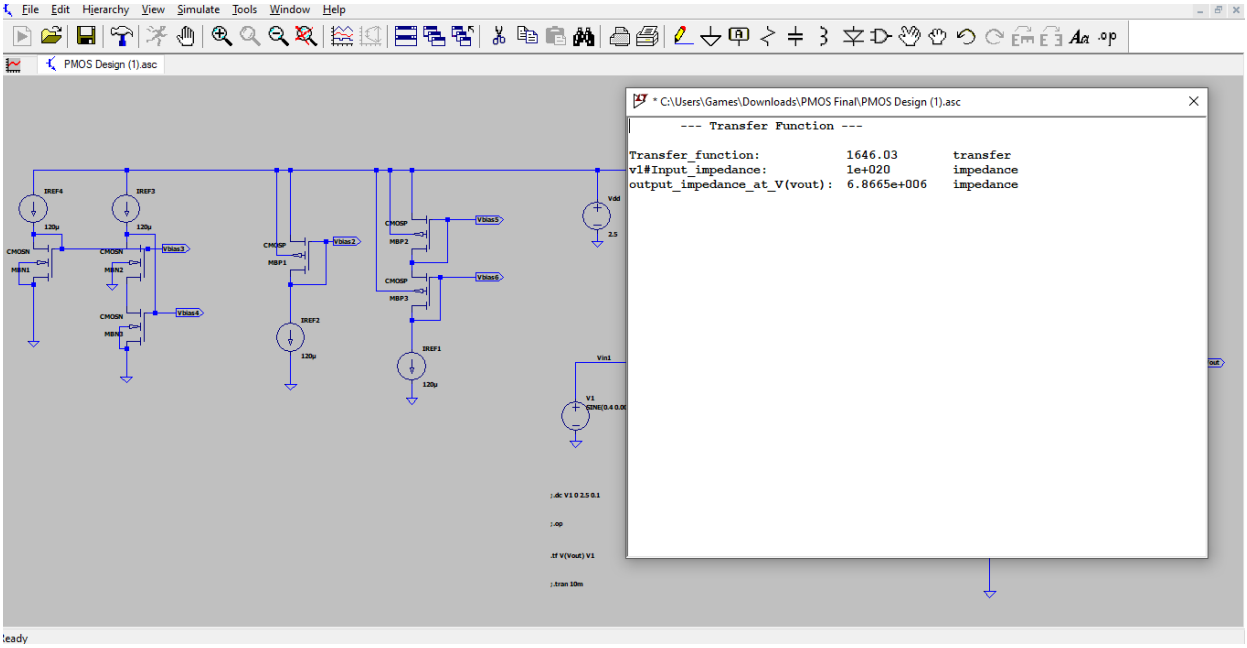

FIGURE 5. - Transfer function output of the designed circuit

The transfer function analysis is also running to confirm the gain, which obtained from the transient analysis. It can be noticed that the gain gotten using both the analysis is similar and is as desired.

Milestone 2

Figure 6 shows the design of two stage op-amp by using the LT-Spice EDA tool-to design the op Amp circuit. The W/L ratios are set in such a way that make all the transistors remain in saturation region. In this design 2 µm gate length is used for all the transistors to bring them in saturation region. For stability purpose we use 1 f and 100 n capacitor at the output of the circuit.

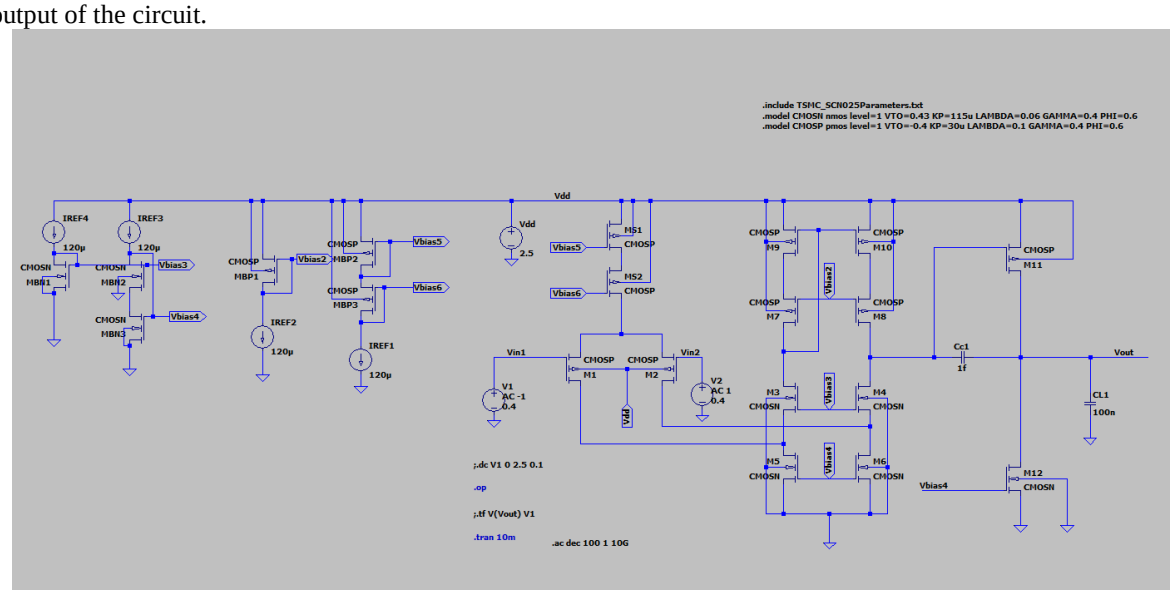

FIGURE 6. - Designed circuit of two stage op amp

Design Specification

The V_{dd} used is 2.5 volt and differential input Vin^{+} and Vin^{-} of 1 volt and for biasing voltage design simple transistor level self-biasing circuit which generates the different biasing voltage. The widths and biasing of the above circuits have

been calculated using the values considered for power dissipation and open loop DC voltage gain (given in the specifications). Table 4 shows the two-stage op amp performance.

Table 4. - Two- stage op amp performance

Parameter	Values
P_D	3.4 mW
A_{vo}	91 dB
GB	10 GB
PM	68°

Power Dissipation

Figure 7 shows the total power consumption analyses.

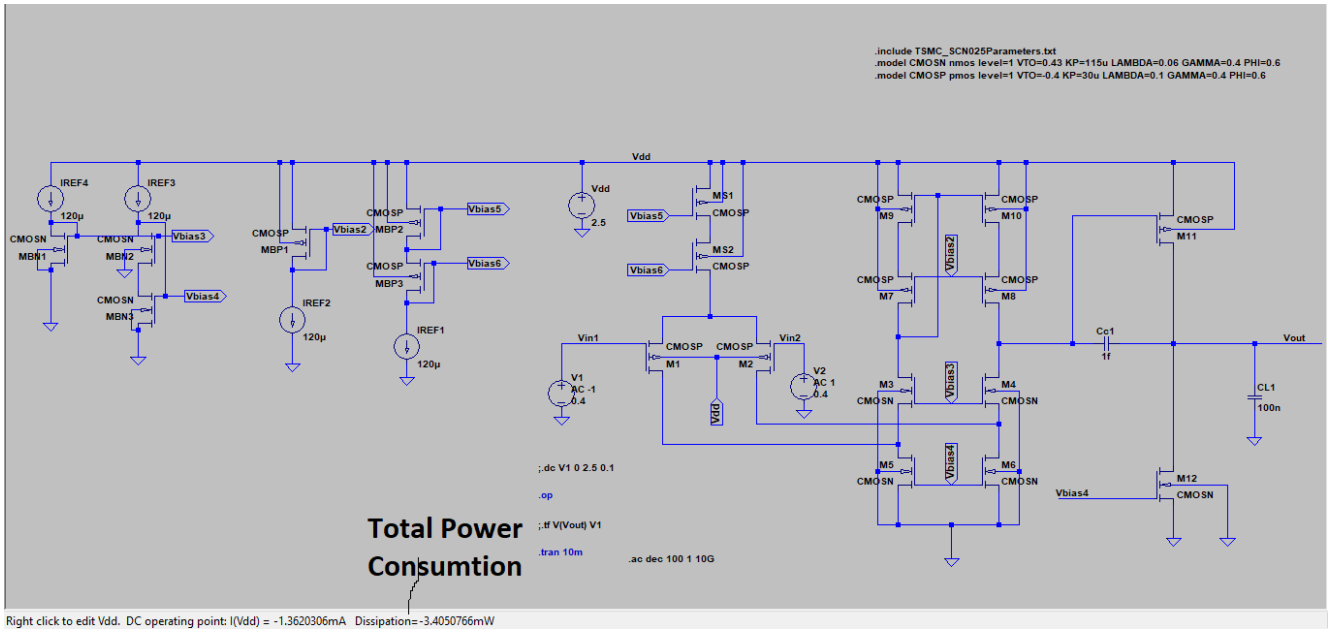

FIGURE 7. - Total power consumption analyses

By using the AC analysis, the current value is got. AC analyses show the op-amp consume about 1.3 milli ampere current

As it is known that P= I*V

$$P = 1.3 \times 2.5 = 3.4\ \mu w \qquad (4)$$

So, it also verifies to the written hand calculations.

The suitable capacitor values chosen for this design are:

Cc = 1 F

Cl = 100 nF

Figure 8, 9 and 10 show the transient plot, transient plot of inputs and bode plot respectively.

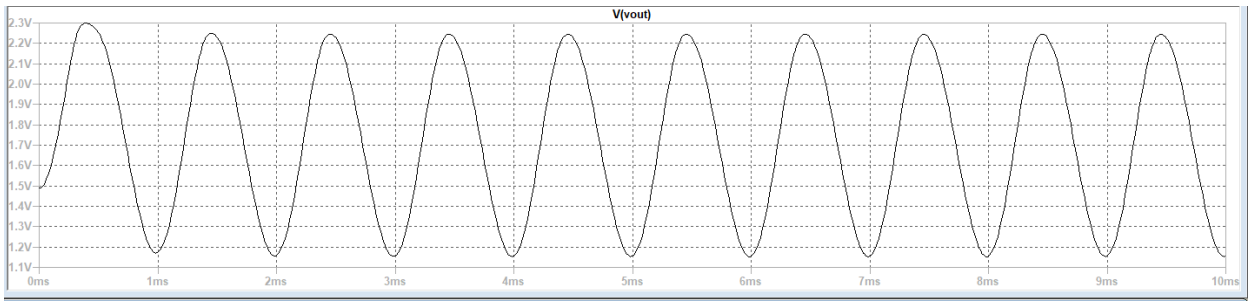

FIGURE 8. - Transient plot

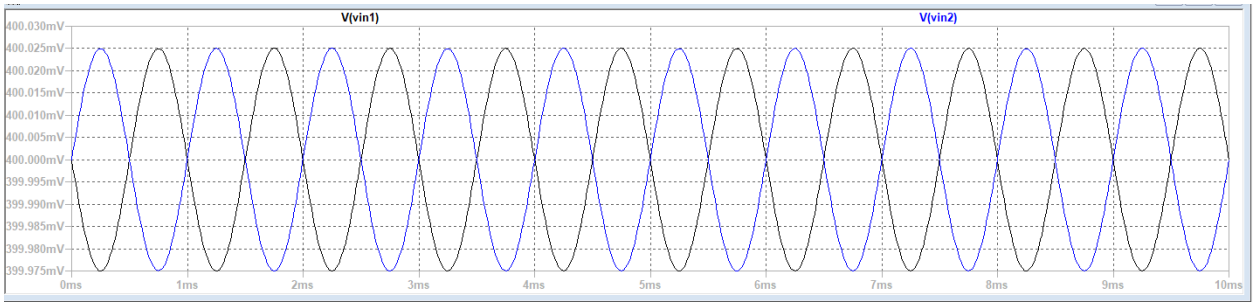

FIGURE 9. - Transient plot of inputs

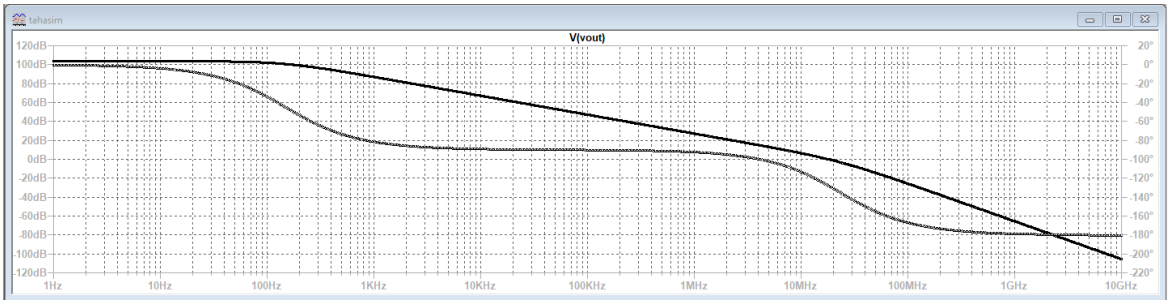

FIGURE 10. - Bode plot

The transient analyses of om-amp are simulated to confirm the gain, which is obtained from the transient analysis. It can be seen that the op-amp achieve 91 dB gain and also 68^{o} gain which are equal to our hand written calculation.

5. CONCLUSION

In milestone 1, all the simulation are done in the LTspice Software tool using TSMC 0.25 µm Technology taking minimum channel length of the transistors are taking as 2 µm. The simulation was run using 2.5 V supply voltages for the fully differential folded cascode op amps in both PMOS input. Thus, getting the high open loop DC voltage gain and high ICMR for the given specifications, it can be observed that the widths of few transistors is needed to change (from the calculated values) to make all the transistors in saturation. This happens because in hand calculations, the lambda term is neglected in current calculation and because of which some of the MOSFETs were in triode region. Therefore, their width has been decreased to bring them in saturation to get required high voltage gain. Thus, from all of the above simulation plots, the correct and required performance of the circuit can be observed.

In milestone 2, two-stage op amp circuit has been designed based on Ltspice simulator. For the calculations, 1 F as a compensation capacitor and 100 nF as a load capacitor have been added to the circuit of one stage op amp that has been designed in milestone 1. In addition to these capacitors 1 F and 100 nF, two transistors types (PMOS – M11) and (NMOS – M_{12}) with a width value W_{11} and W_{12} of about (888.88 and 231.88) µm have been added to the designed circuit respectively. Two parameters of the designed circuit were Zero (z)= 10 GB, and Phase margin (PM= 68 ^{o}). Two other parameters of the designed circuit such as power dissipation PD has been calculated of about (PD= 3.4 mW). The obtained output gain of this circuit was Avo= 91 dB, this result revealed that the design has a high gain.

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CONFLICTS OF INTEREST

The authors declare no conflict of interest

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