Al-Salam Journal for Engineering and Technology
Journal Homepage: http://journal.alsalam.edu.iq/index.php/ajest
e-ISSN: 2790-4822p-ISSN: 2958-0862

Design For Testability Method To Sequential Circuit

Taha Rashid[1,2], Muhammad Naziiruddin bin Hamzah[2], Mohammed RASHEED[3, 4] *, Ahmed Shawki Jaber[5], Mohammed Abdelhadi Sarhan[5], Mustafa Nuhad Al-Darraji[6], Tarek Saidani[7], Ahmed Rashid[1]

[1]College of Arts, Al-Iraqia University, Baghdad, Iraq
[2]Computer and Microelectronic Systems, Faculty of Engineering, Universiti Teknologi Malaysia (UTM), Skudai 81310, Johor Bahru, Malaysia
[3]Applied Sciences Department, University of Technology, Baghdad, Iraq
[4]MOLTECH Anjou, Universite d'Angers/UMR CNRS 6200, 2, Bd Lavoisier, 49045 Angers, France
[5]Mathematics Science Department, College of Science, Mustansiriyah University, Baghdad, Iraq
[6]Department of Biology, College of Science, University Of Al-Anbar, Anbar, Iraq
[7]Department of Physics, Akli Mohaned Oulhadj University of Bouira, Bouira, 10000, Algeria

*Corresponding Author: Mohammed RASHEED

DOI: https://doi.org/10.55145/ajest.2023.02.02.002
Received December 2022; Accepted February 2023; Available online February 2023

ABSTRACT: As the complexity of logic devices increased, it required more time and effort to manually design and verify tests, it was difficult to estimate test coverage, and the tests ran too slowly. This method is known as functional testing. Therefore, the industry adopted a design for test (DFT) strategy in which the design was updated to make testing simpler. In this work, a full scan testability method is going to be implemented to a sequential circuit (CUT). The CUT consists of at 6 D flip-flops and 10 logic gates. This CUT was designed using quartus prime software. The following steps are going to be implemented in this work: First, simulate the fault free circuit. Second, three faults were injected and tested to check if they can be detected or not. Finally, analyze the obtained results in terms of (what is the test pattern needed, how the fault can be observed at output).

Keywords: Design for testability (DFT), sequential Circuit, flip-flop, circuit under test (CUT), full scan

1. INTRODUCTION

As a result of semiconductors, the electronics sector is making constant progress. The semiconductor industry has been able to keep up with rising performance-capacity expectations because of the advent of new technologies, particularly nanometre technologies with 14 nm or smaller geometries. The industry's long-term outlook has been improved as a result of this [1]. The problem is that with new technology come new difficulties. Several types of mistakes become more likely as die sizes decrease. Incorrect ICs are a major problem. Some problems that might occur during chip production are listed below [2].

Maintenance Issue: In the event of a future breakdown, precise fault coordinates will be necessary for servicing and repair. Due to shrinking PCB sizes, multimeter testing is becoming obsolete. Moreover, as we go towards SoC (System on Chip) architecture, the modular design is becoming less useful, which in turn increases the cost of maintenance [3].

Density Issue: The development of deep-submicron design technology has added a great deal of complexity to the fabrication process. It's easy to see this trend in the shrinking and thinning of design components, which are drawing closer to one another. The transistor count on today's VLSI chips is in the billions. Consequently, there is a considerable potential for a short circuit to occur between two wires, or for a very thin wire to break. To name just a

*Corresponding author: rasheed.mohammed40@yahoo.com

few, these may be the causes of mistakes. The point is that numerous such mistakes might arise throughout the planning and production phases. Failure is thus more likely the higher the density [4].

Software Issue: Additionally, inaccuracies in the translation process are possible owing to flaws in the CAD software tools used to design the chip, which may occur at any stage of the process from manufacture to translation [5].

Solutions to these problems is design for testability (DFT) Simply said, Design for testability is a method of chip design that incorporates extra circuitry to make testing the chip easier and cheaper [6]. Alternatively, embedded functions may be evaluated with the help of Design-for-testability methodologies, which increase the internal nodes' controllability and observability [7].

The cost of testing is not negligible. Present day microprocessors have more than 1000 pins. The number of features they provide is staggering. If even one transistor on a chip fails, the whole chip is useless and must be thrown away. To put it simply, the customers do not count on manufacturers to provide them with defective chips. However, it might be difficult to find a single faulty transistor among billions. We may have to try out every feature in every imaginable permutation. The time-to-market for the chips might be so long if testing is conducted in that manner. So, we use a specific procedure to upgrade these chips. Design for Testability (or DFT) is the acronym for this approach. Furthermore, it enhances a chip with the property of "testability" [8].

The problem of testing sequential circuits may be overcome with the help of DFT. Unfortunately, testing sequential circuits may be challenging. Because in addition to the flip-flops, there are also clocks to consider [9]. In contrast to combinational circuits, the output of sequential circuits cannot be determined by only examining the inputs. By virtue of flip-flops, sequential circuits have limited states. Additionally, the production relies on the condition of the equipment. Internal flip-flops are difficult to regulate and witness outside [10-22]. Therefore, the state machines cannot be tested without being started with a known value. In addition to the normal circuitry, we require a special set of characteristics to initialize them. DFT permits the addition of this feature to a sequential circuit, allowing us to test it. In this paper, DFT using full scan method is going to be implemented for a circuit that consists of 10 logic gates, and 6 Flipflops.

2. METHOD

In this section, 10 logic gates, 6 (2 to1) multiplexers as well as 6 D flipflops (FF1, FF2, FF3, FF4, FF5, FF6) were connected properly to implement full scan method. The primary inputs are (A, B, C, D, E, F), SI is the pin used to initialize the flipflops with the desired values, select pin is used to select between test mode or normal mode (Select=1 for test mode, select=0 for normal mode), CLK pin is the clock. Z is the primary output, and finally SO is the scan output as shown in Figure 1.

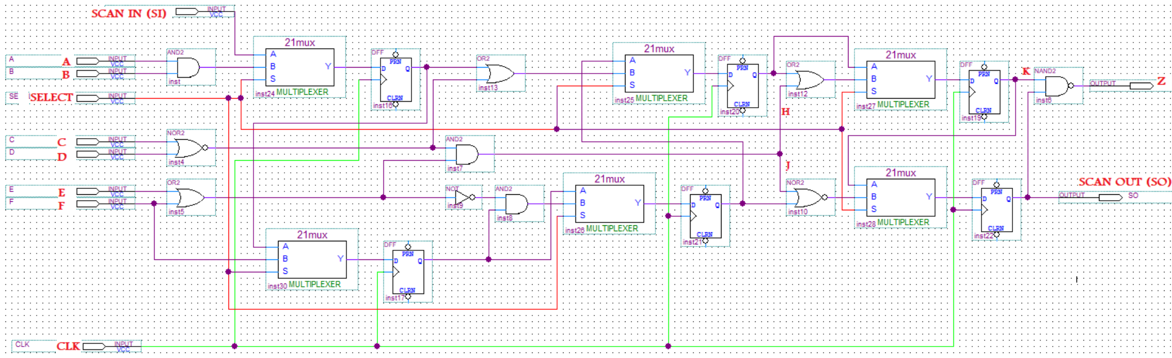

FIGURE 1. - **Circuit under test**

First of all, the Flipflops, primary inputs (A, B, C, D, E, F), SI pin, and Select pin need to be initialized and after that the circuit is simulated to get the fault free circuit's wave form result which will be used for a comparison with faulty circuit.

3. RESULTS AND DISCUSSION

3.1 H STUCK at 1

In this case we are injecting a fault in CUT by connecting H input to VCC as shown in Figure 2, this line will be always stuck at 1. To propagate this fault, the test pattern used is for {A, B, C, D, E, F, FF1, FF2, FF3, FF4, FF5, FF6} is {0,0,0,0,0,0,0,0,0,0,0,1} respectively, as shown in Table 1, to propagate the fault then the fault will be propagated

through FF5 and FF6 and through Z. The fault was detected at Z pin after 7 clock cycles, because the original value of Z pin in fault free circuit was (Z=1), while we get (Z=0) in faulty circuit as shown in Figure 3, Figure 4 and Table 2.

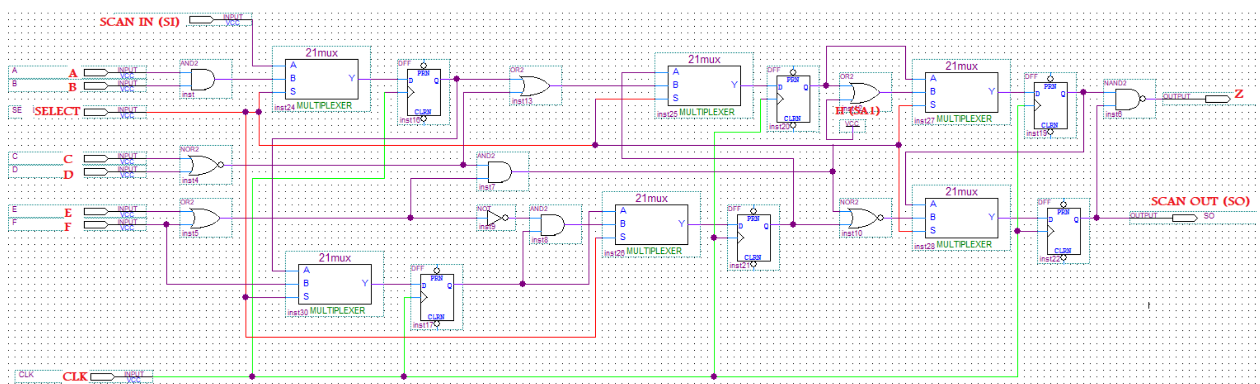

FIGURE 2. - H stuck at 1

Table 1. - Test pattern used for H stuck at 1.

P_{in}	A	B	C	D	E	F	FF1	FF2	FF3	FF4	FF5	FF6
Input	0	0	0	0	0	0	0	0	0	0	0	1

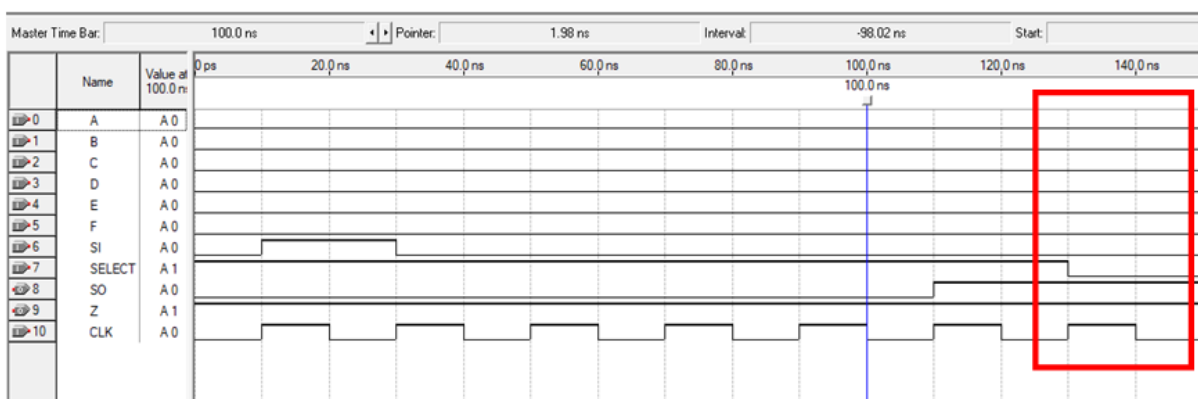

FIGURE 3. - Fault Free waveform (H stuck at 1)

FIGURE 4. - H stuck at 1 simulation waveform

Table 2. - fault free circuit output compared to faulty circuit output (H stuck at 1).

Fault free circuit		Faulty circuit		Number of clock cycle needed
Primary output (Z)	**Scan out (SO)**	**Primary output (Z)**	**Scan out (SO)**	
1	1	0	1	7

3.2 J STUCK at 1

In this case we are injecting a fault in CUT by connecting H input to VCC as shown in Figure 3, this line will be always stuck at 1. To propagate this fault, the test pattern used is {A, B, C, D, E, F, FF1, FF2, FF3, FF4, FF5, FF6} is {0,0,0,0,0,0,0,0,0,0,0,1} respectively, as shown in Table 3, to propagate the fault then the fault will be propagated through and FF6 and through Z. The fault was detected at scan out pin after 7 clock cycles, because the original value of scan out pin in fault free circuit was Scan out (SO=1), while we get scan out (SO=0) in faulty circuit as shown in Figure 6, Figure 7 and Table 4.

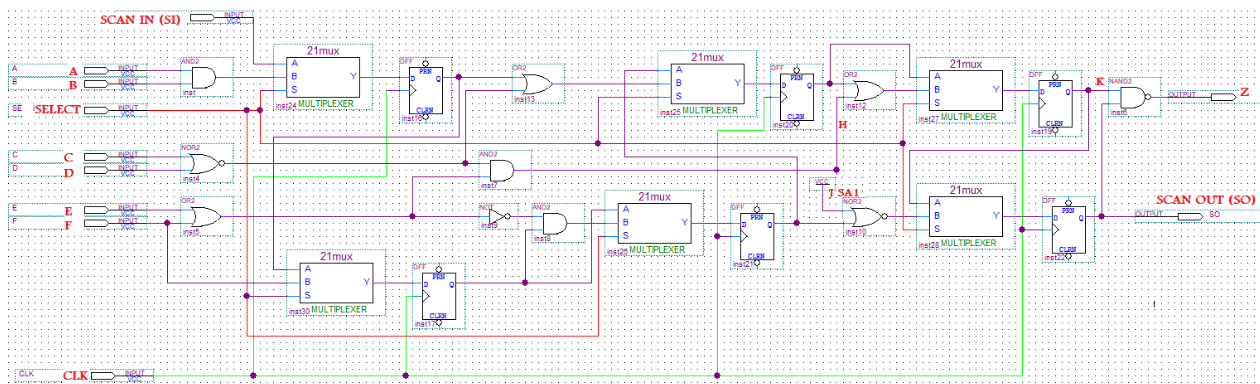

FIGURE 5. - J stuck at 1

Table 3. - Test pattern used for J stuck at 1.

P_{in}	A	B	C	D	E	F	FF1	FF2	FF3	FF4	FF5	FF6
Input	0	0	0	0	0	0	0	0	0	0	0	1

FIGURE 6. - Fault Free simulation waveform (J stuck at 1)

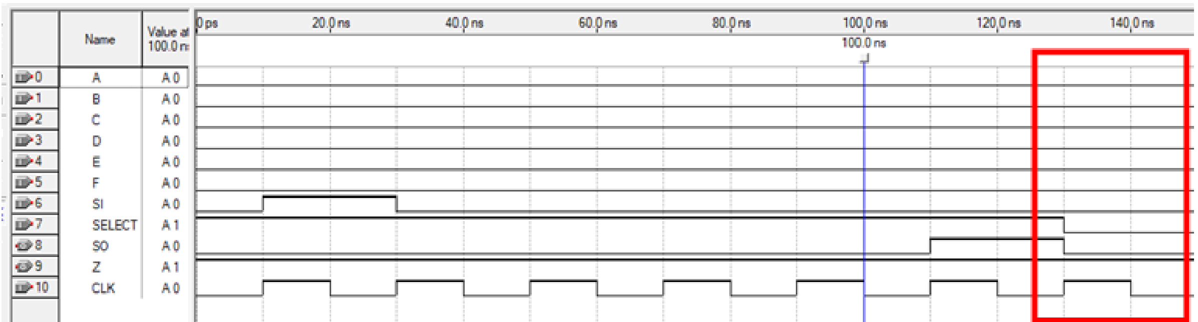

FIGURE 7. - J stuck at 1 simulation waveform

Table 4. - fault free circuit output compared to faulty circuit output (J stuck at 1).

Fault free circuit		Faulty circuit		Number of clock cycle needed
Primary output (Z)	Scan out (SO)	Primary output (Z)	Scan out (SO)	
1	1	1	0	7

3.3 K STUCK at 0

In this case we are injecting a fault in CUT by connecting H input to VCC as shown in Figure 3, this line will be always stuck at 1. To propagate this fault, the test pattern used is {A, B, C, D, E, F, FF1, FF2, FF3, FF4, FF5, FF6} is {0,0,0,0,0,0,0,0,0,1,1,1} respectively, as shown in Table 5, to propagate the fault then the fault will be propagated through and FF6 and through Z. The fault was detected at Z pin after 6 clock cycles, because the original value of scan out pin in fault free circuit was (Z=1), while we get scan out (Z=0) in faulty circuit as shown in Figure 9, Figure 10 and Table 6.

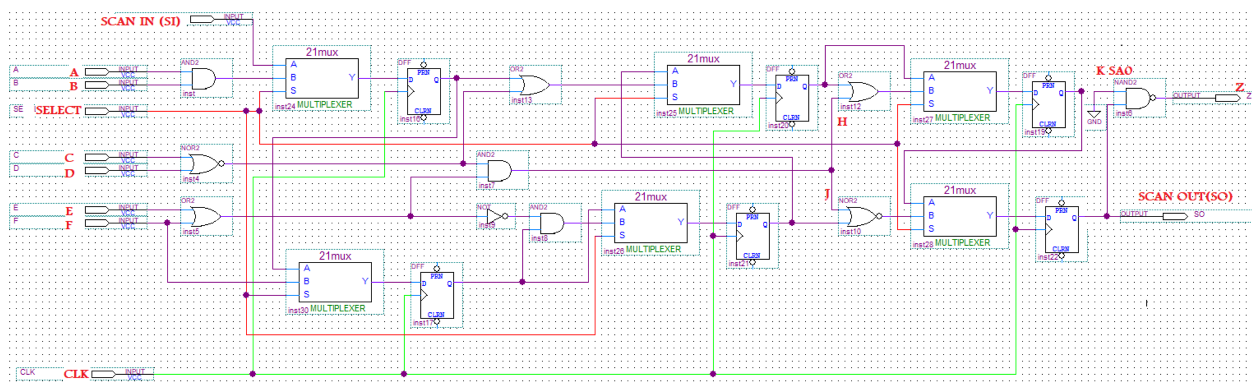

FIGURE 8. - K stuck at 0

Table 5. - Test pattern used for K stuck at 0.

P_{in}	A	B	C	D	E	F	FF1	FF2	FF3	FF4	FF5	FF6
Input	0	0	0	0	0	0	0	0	0	1	1	1

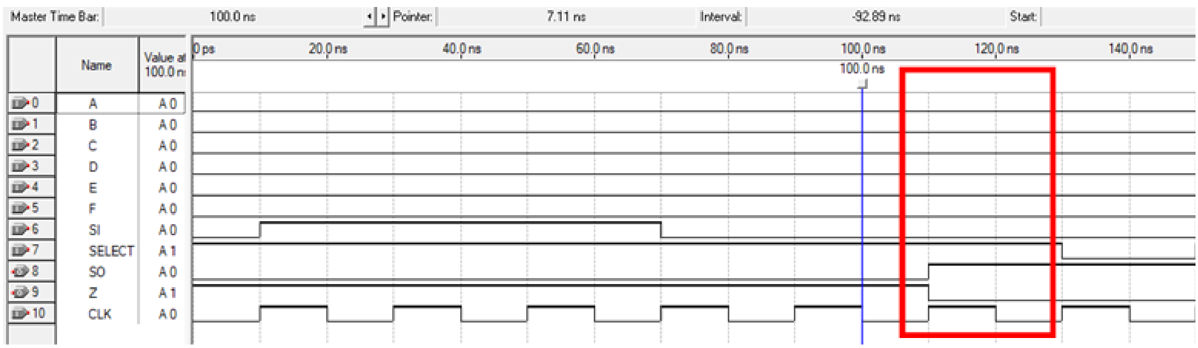

FIGURE 9. - Fault Free simulation waveform (K stuck at 0).

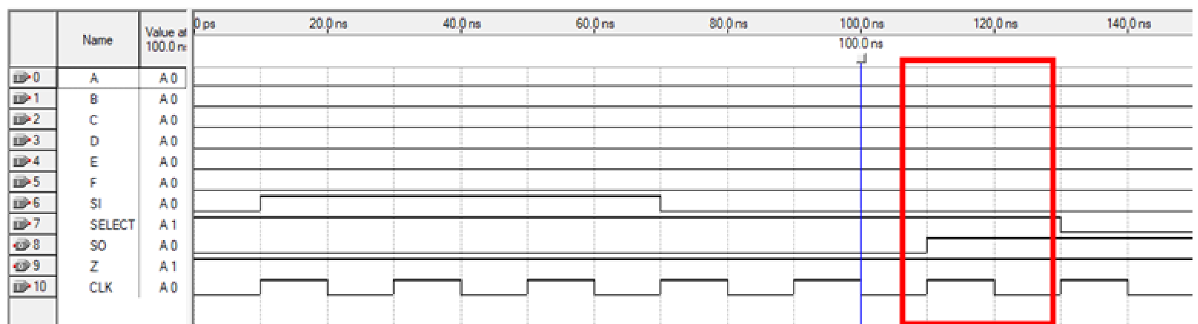

FIGURE 9. - K stuck at 0 simulation waveform

Table 6. - fault free circuit output compared to faulty circuit output (K stuck at 0).

Fault free circuit		Faulty circuit		Number of clock cycle needed
Primary output (Z)	Scan out (SO)	Primary output (Z)	Scan out (SO)	
0	1	1	1	6

Area Overhead

$$Area\ overhead\ = \left[4 \times \frac{n_{sff}}{n_g + n_{sff}}\right] \times 100\%$$

$$Flip\ flop = 6,\quad Gates = 10$$

$$n_g = 10,\qquad n_{sff} = 6,\qquad 1\ flipflop = 10\ gates$$

$$Area\ overhead = \left[\frac{4 \times 6}{(10 + (6 \times 10))}\right] \times 100\%$$

$$= \left[\frac{24}{70}\right] \times 100\%$$

$$= 34.29\%$$

From the results obtained there are a few observations can be made. For H stuck at 1 the test pattern used for {A, B, C, D, E, F, FF1, FF2, FF3, FF4, FF5, FF6} was {0,0,0,0,0,0,0,0,0,0,0,1}. However, all inputs A, B, C, D, E, F is actually unknown X since we do not care its value since it does not affect the propagation of the fault through the scan out and output Z, however for the sake of the simulation the value unknown cannot be set because it will give an error thus in the simulation all the unknown will just be set to 0. In order the observe whether the fault has been propagated or not the scan out pin and output z pin was observed and to ensure that the fault is propagated we need to make sure scan out pin an output z pin is D' for H stuck at 1 and to do this the circuit was simulated with the test pattern mention, {0,0,0,0,0,0,0,0,0,0,0,1} for H stuck at 1 then by using the same test pattern the circuit was simulated for fault free where the fault was removed and the output waveform is compared between fault free and faulty. From the output waveform we can observe at the 7th clock cycle the output Z is 1 for fault free and 0 for faulty circuit while the scan out pin is the same which is 1 for both faulty and fault free thus the fault can be observed at Z and not at scan out. This is due to when the flip flop is initialized for 6 clock cycle then the D' is propagated through FF5 which adds another clock cycle during normal mode however the fault is still not propagate to primary output Z or scan out because the output for z and scan out pin is still the same for fault free and faulty so the fault is then propagate through the NAND gate thus is why we can observe the output at Z as shown in the waveform but we do not need to add another clock cycle because the fault went through a logic gate and not a flip flop. So, the total clock cycle used for H stuck at 1 is 7 clock cycle.

For J stuck at 1 the test pattern uses for {A, B, C, D, E, F, FF1, FF2, FF3, FF4, FF5, FF6} was {0,0,0,0,0,0,0,0,0,0,0,1}. The same process was done which was the circuit simulated using the test pattern for fault J stuck at 1 and then circuit was simulated using the same test pattern for fault free circuit. Then we compare the waveforms. For J stuck at 1 the output Z is 1 for faulty and fault free while the scan out pin is 0 for faulty circuit and 1 for fault free thus the fault can be detected at the scan out pin. After the flip flop was initialized for 6 clock cycle then the fault is verified to be propagated through the FF6 in normal mode since scan out is 0 for faulty and 1 for fault free which adds another clock cycle. Since the fault is already propagated through the scan out, we do not need to propagate the fault through Z. So, the total clock cycle used to detect J stuck at 1 is 7 clock cycle.

Lastly for K stuck at 0 the test pattern used was {A, B, C, D, E, F, FF1, FF2, FF3, FF4, FF5, FF6} was {0,0,0,0,0,0,0,0,0,1,1,1}. In order to activate the fault FF4 and FF5 must be 1 to activate the fault and the FF6 must be 1 so that the fault can be propagated through the NAND gate and to Z. The circuit was simulated using the test pattern for fault free and K stuck at 0. From the output waveform we can observe that the primary output Z is 1 for faulty and 0 for fault free circuit which means that the fault can be observed at primary output Z and not the scan out pin. The fault can be observed during the 6th clock cycle, this is due to when the Flip flop has been initialized for 6 clock cycle then the fault is propagated to Z during normal mode, however another clock cycle is not needed since the fault is propagated through a logic gate in normal mode.

4. CONCLUSION

Manually creating and validating tests for ever more sophisticated logic devices was too time-consuming, test coverage was difficult to assess, and test runs took too long. Functional testing describes the method used. So, businesses adopted a design for test (DFT) strategy, wherein designs were altered to facilitate testing. In this paper, the full scan approach of design for testability to a sequential circuit (CUT) has been done. 6 D flip-flops and 10 logic gates make up the CUT. The Quartus prime program was used to create this CUT. Following are the procedures that was used to complete this task: A perfect circuit simulation must first be performed. Second, the system's ability to identify problems was evaluated by injecting three different types of errors. As the last step, evaluate the gathered data in (what is the test pattern needed, and how the fault can be observed at output). It is concluded that all faults can be detected using the given test patterns.

Funding

None

ACKNOWLEDGEMENT

We are grateful to Al-Iraqi University, University of Technology and Universite d'Angers for providing support to accomplish this work.

CONFLICTS OF INTEREST

The authors declare no conflict of interest

REFERENCES

[1] B. Garg and G. K. Sharma, "ACM: An Energy-Efficient Accuracy Configurable Multiplier for Error-Resilient Applications," Journal of Electronic Testing, vol. 33, no. 4, pp. 479–489, Jun. 2017, doi: 10.1007/s10836-017-5667-8.

[2] T. Le, "Audit Quality Inputs and Financial Statement Reliability," SSRN Electronic Journal, 2018, doi: 10.2139/ssrn.3195245.

[3] H. Hu and S. S. Sapatnekar, "Efficient inductance extraction using circuit-aware techniques," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 10, no. 6, pp. 746–761, Dec. 2002, doi: 10.1109/tvlsi.2002.808455.

[4] S. Hain and T. Bertelshofer, "Efficiently Designed SiC Power Electronics for Electric Drives," ATZelectronics worldwide, vol. 15, no. 7–8, pp. 58–61, Jul. 2020, doi: 10.1007/s38314-020-0223-1.

[5] Fong Pong and M. Dubois, "Formal automatic verification of cache coherence in multiprocessors with relaxed memory models," IEEE Transactions on Parallel and Distributed Systems, vol. 11, no. 9, pp. 989–1006, 2000, doi: 10.1109/71.879780.

[6] A. S. Abu-Issa, "Energy-Efficient Scheme for Multiple Scan-Chains BIST Using Weight-Based Segmentation," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 3, pp. 361–365, Mar. 2018, doi: 10.1109/tcsii.2016.2617160.

[7] G. Arya, "Performance Analysis of Arithmetic Logic Unit with Reversible Logic," International Journal of Advanced Trends in Computer Science and Engineering, vol. 9, no. 4, pp. 6585–6590, Aug. 2020, doi: 10.30534/ijatcse/2020/348942020.

[8] H. B. Pan, M. X. Song, X. Jin, and J. H. Yin, "Full Scan Structure Application in the Design of 16 Bit MCU," Advanced Materials Research, vol. 981, pp. 78–81, Jul. 2014, doi: 10.4028/www.scientific.net/amr.981.78.

[9] M. Rasheed, O. Alabdali, S. Shihab, A. Rashid, and T. Rashid, “On the Solution of Nonlinear Equation for Photovoltaic Cell Using New Iterative Algorithms,” Journal of Physics: Conference Series, vol. 1999, no. 1, p. 012078, Sep. 2021, doi: 10.1088/1742-6596/1999/1/012078.

[10] S. Potluri, P. Pop, and J. Madsen, “Design-for-Testability of On-Chip Control in mVLSI Biochips,” IEEE Design & Test, vol. 36, no. 1, pp. 48–56, Feb. 2019, doi: 10.1109/mdat.2018.2873448.

[11] E. Ph. Pevtsov, T. A. Demenkova, and A. A. Shnyakin, “Design for Testability of Integrated Circuits and Project Protection Difficulties,” Russian Technological Journal, vol. 7, no. 4, pp. 60–70, Aug. 2019, doi: 10.32362/2500-316x-2019-7-4-60-70.

[12] A. H. Ali, A. S. Jaber, M. T. Yaseen, M. Rasheed, O. Bazighifan, and T. A. Nofal, “A Comparison of Finite Difference and Finite Volume Methods with Numerical Simulations: Burgers Equation Model,” Complexity, vol. 2022, pp. 1–9, Jun. 2022, doi: 10.1155/2022/9367638.

[13] D. Bouras, M. Rasheed, R. Barille, and M. N. Aldaraji, “Efficiency of adding DD3+(Li/Mg) composite to plants and their fibers during the process of filtering solutions of toxic organic dyes,” Optical Materials, vol. 131, p. 112725, Sep. 2022, doi: 10.1016/j.optmat.2022.112725.

[14] M. Darraji, L. Saqban, T. Mutar, M. Rasheed, and A. Hussein, “Association of Candidate Genes Polymorphisms in Iraqi Patients with Chronic Kidney Disease,” Journal of Advanced Biotechnology and Experimental Therapeutics, vol. 6, no. 1, p. 687, 2022, doi: 10.5455/jabet.2022.d147.

[15] N. Assoudi et al., “Comparative examination of the physical parameters of the sol gel produced compounds La0.5Ag0.1Ca0.4MnO3 and La0.6Ca0.3Ag0.1MnO3,” Optical and Quantum Electronics, vol. 54, no. 9, Jul. 2022, doi: 10.1007/s11082-022-03927-x.

[16] M. Al-Darraji, S. Jasim, O. Salah Aldeen, A. Ghasemian, and M. Rasheed, “The Effect of LL37 Antimicrobial Peptide on FOXE1 and lncRNA PTCSC 2 Genes Expression in Colorectal Cancer (CRC) and Normal Cells,” Asian Pacific Journal of Cancer Prevention, vol. 23, no. 10, pp. 3437–3442, Oct. 2022, doi: 10.31557/apjcp.2022.23.10.3437.

[17] D. Bouras, M. Fellah, A. Mecif, R. Barillé, A. Obrosov, and M. Rasheed, “High photocatalytic capacity of porous ceramic-based powder doped with MgO,” Journal of the Korean Ceramic Society, Oct. 2022, doi: 10.1007/s43207-022-00254-5.

[18] Bouras and M. Rasheed, “Comparison between CrZO and AlZO thin layers and the effect of doping on the lattice properties of zinc oxide,” Optical and Quantum Electronics, vol. 54, no. 12, Oct. 2022, doi: 10.1007/s11082-022-04161-1.

[19] M. A. Sarhan, S. Shihab, B. E. Kashem, and M. Rasheed, “New Exact Operational Shifted Pell Matrices and Their Application in Astrophysics,” Journal of Physics: Conference Series, vol. 1879, no. 2, p. 022122, May 2021, doi: 10.1088/1742-6596/1879/2/022122.

[20] M. Rasheed, M. Nuhad Al-Darraji, S. Shihab, A. Rashid, and T. Rashid, “The numerical Calculations of Single-Diode Solar Cell Modeling Parameters,” Journal of Physics: Conference Series, vol. 1963, no. 1, p. 012058, Jul. 2021, doi: 10.1088/1742-6596/1963/1/012058.

[21] M. Rasheed, M. N. Al-Darraji, S. Shihab, A. Rashid, and T. Rashid, “Solar PV Modelling and Parameter Extraction Using Iterative Algorithms,” Journal of Physics: Conference Series, vol. 1963, no. 1, p. 012059, Jul. 2021, doi: 10.1088/1742-6596/1963/1/012059.

[22] T. Rashid and M. M. Mokji, “Low-Resolution Image Classification of Cracked Concrete Surface Using Decision Tree Technique,” Lecture Notes in Electrical Engineering, pp. 641–649, 2022, doi: 10.1007/978-981-19-3923-5_55.