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Design and simulation of high gain two stage operational amplifier using 180n technology with Nano range

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ABSTRACT: In this study, two different types of op-amps were designed and tested at a lower voltage. These op-amps use less power and can be used at a lower voltage than traditional op-amps, which makes them a good option for certain applications. The designer predicted that the power output would be high when there is a high voltage supply, and LT Spice software was used to analyze the design. Today, low-powered operational amplifiers are in high demand for many applications, such as in medical and communication systems. Some of the reasons why op-amps are in high demand are because they are versatile and have a wide range of applications. Additionally, they are often less expensive than more powerful amplifiers, which makes them a good option for certain applications. This op-amp has a good phase margin, so it can handle large loads with ease. It was created using a 180-millisecond process and CMOS technology. A 3-pF compensation capacitor and a 10-pF load capacitor are suitable for it, as the op-amp has a phase margin of 90.84 degrees...

Keywords: op map, 180 nm, ltspice, gain, cmos

1. INTRODUCTION

An operational amplifier is a versatile and essential building block when designing analog or mixed signal circuits. It can be used for a variety of applications, such as communication and medical systems [1], and has a variety of functions. An operational amplifier, like most electronic devices, has a forward gain (the amplification of the input signal) and a feedback gain (the amplification of the output signal after the amplifier has corrected for feedback). The feedback gain is larger than the forward gain, so the operational amplifier's amplification is effectively independent of the amplifier's gain. However, negative feedback is necessary in order to create a closed-loop transfer function, so the amplifier's gain is effectively dependent on the amplifier's gain. FIGURE 1: The symbol for op-amps.

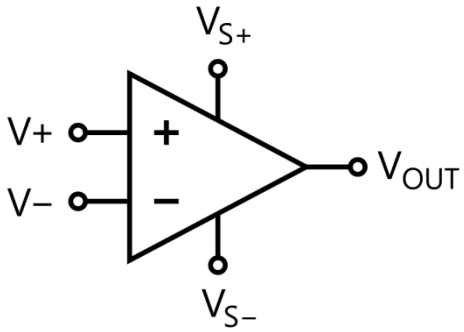

FIGURE 1. - The symbol for op-amps

The advantage of op-amps is that they are able to amplify a million times larger than what is possible with other circuit types. Ideal op-amps have infinite input impedance and infinite differential voltage gain, but in reality, they approach these values only.

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There are a variety of applications for op-amps because of their linear device characteristic. Operational amplifiers are used to amplify signals, and they can be used to perform various arithmetic operations. The design of operational amplifiers is increasingly difficult, as the channel lengths of CMOS technology transistors have decreased. There are various feedback components that can be used to improve the amplifier's performance.[2].

In the world of computers, amplifiers that carry out different mathematical operations are known as operational amplifiers. It has been discovered that operational amplifiers with negative feedback are especially useful for defining amplifiers that carry out a variety of mathematical operations. The addition of negative feedback to a high gain amplifier circuit results in an accurate gain characteristic that is only reliant on the feedback added. This can be accomplished using an op-amp circuit, which is versatile for a variety of tasks [1].

When working with devices that have short channel lengths, op amp design faces unique difficulties. There are several implementation options available to us because of recent advancements in new approaches and technology One problem with two-stage CMOS operational amplifiers is that their output signals can have two very strong electric fields that can be difficult to keep stable. This can lead to problems like the amplifier generating its own oscillations instead of transforming the input signal into an output signal [12]. Two-stage op amps are used in these circumstances because they have variable gain and output power. This architecture allows for high gain in the first stage and significant swing in the second level. In contrast, cascaded op amps need gain and swing to be controlled separately, which can be a problem in certain situations [2].

Two-stage op amps can be used to increase the gain and swing of a signal. The gain increase is only around 5-15 dB, but this is helpful in some applications. Additionally, the second stage can offer greater output power variation, which is helpful in certain applications.[12].

2. BASICS OF TWO-STAGE OPERATIONAL AMPLIFIER

The diagram in Figure 2 shows a two-stage operational amplifier with differential and common-source amplifiers. The differential amplifier amplifies the difference in voltage between the input ports, while the common-source amplifier amplifies the common voltage between the input ports [13]. The common-source amplifier supplies the high output voltage required to boost the gain, while the differential amplifier amplifies the difference between the two input voltages. This is why the differential amplifier is able to boost the voltage difference between the two inputs, rather than reducing the voltage that is shared by the two inputs. Either an inverting voltage (V-), or a non-inverting voltage (V+) can be used as inputs. Depending on the input voltages, the output can be either single-ended or differential. The differential amplifier output is used as the input to a common-source amplifier, which provides additional gain.

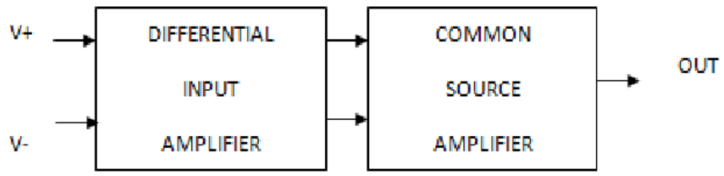

FIGURE 2. - A two-stage op-amp block diagram is shown. In the first stage, an op-amp amplifies the input signal. In the second stage, the amplified signal is applied to the output

3. A TWO-STAGE OPEARTIONAL AMPLIFIER SCHEMATIC DESIGN

In this project, a two-stage CMOS operational amplifier is being created using 180 nm technology. The bias chains section consisted of three chains, each with a different bias voltage. The differential gain stage consisted of two stages, each with a different gain voltage. The gain stage allowed for a large output swing, which helped the differential circuit stage create even more gain. as shown in Figure 3.

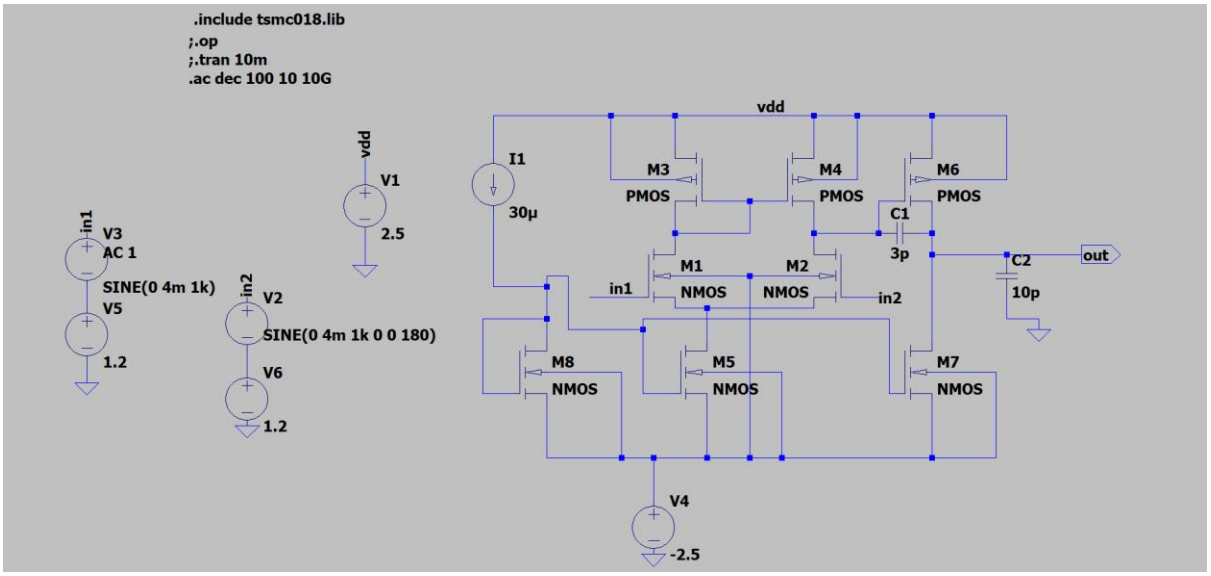

FIGURE 3. - A two-stage operational amplifier schematic design can be used to improve the performance of an amplifier

The operational amplifier's differential stage is made up of NMOS1, NMOS2, PMOS3, and PMOS4 transistors. Each pair of transistors performs a small amount of amplification. The NMOS1 and NMOS2 gates are the transistors' inverting and non-inverting inputs, while the input transistor resistance and PMOS3 and PMOS4 are the main resistances that make up the amplifier's output power.[3]. Active mirroring PMOS devices can help to increase the current rejection factor of a differential amplifier. The currents of NMOS1 and PMOS3 are identical because NMOS1 is reflected from PMOS3, and NMOS2 and PMOS4 are equal because PMOS4 is subtracted from NMOS2's current [14].

The current loading inverter is the second stage, which is made up of the PMOS6 and NMOS7 transistors. A popular source arrangement is when PMOS6 amplifies the output signal from the NMOS2 drain [4]. Four transistors are also used to accomplish the operational amplifier's biasing. The bias chain that controls NMOS5 and NMOS8 transistors causes them to draw a particular amount of current in response to the gate-source voltage. The first stage's output is coupled with the trimming capacitor (CC). Its job was to shift the output pole away from the source and lower the dominant pole's frequency [5]. The operational amplifier's output was linked to the charging capacitor.

The LTspice tool was used to design the circuit, and LTspice was also used to write the netlist code. From LTSpice, waveforms are obtained. 8-transistor, two-stage operational amplifier circuit with LTspice field-effect transistors NM0s1 and NMos2 as well as PM0s3, PMOs4, and NMos4 are used to create the differential amplifier. According to the schematic, the common-source amplifier circuit consists of PMOS6 and NMOS7 FETs. NMos5 and NMos8 give biasing. To prevent op-amp clipping and provide the signals with a much wider range, we tune the amplifier to a certain value. A two-stage CMOS amplifier is created when these two circuits are combined.

4. DESGIN AND SIMULATION OF TWO STAGE OP-AMP WITH CMOS TECHNOLOGY

4.1 DESGIN PRODUCER OF TWO STAGE OP AMP (STEPS) FROM THESE QUESTIONS [6]

Step 1 calculate minimum of capacitor (CC)

$$Cc \geq 0{,}22\times\ CL \approx Cc \geq 0{,}22\times\ 10p = 2.2\ pf \approx 3\ pf \quad (1)$$

Step 2 calculate I5 for noms 5

$$I5 = selw\ rate\ \times\ Cc \equiv 3\ u\ \times\ 3\ p\ = 30\ uA \quad (2)$$

Step 3 design size of m3 and m4 pmos transistor using ICMR+

$$\frac{W3}{L3}=\frac{W4}{L4}=\frac{Id5}{up\,cox(vdd-ICMR+\ -Vth3\max+Vth1min)^2}$$

Vth3max= 0.7+0.15= 0.85 and Vth1min= 0.7-0.15=0.5 (4)

$$\frac{W3}{L3}=\frac{W4}{L4}=\frac{30u}{50\,u(2.5-2-\ 0.85+0.55)^2}\approx\frac{2700n}{180n}$$

Step 4 design size of m1 and m2 noms transistor

$$\mathrm{gm1}=\mathrm{GBW}\times\mathrm{Cc}\times2\pi=3\mathrm{MHz}\times3\ \mathrm{pf}\times2\pi=94.25\mathrm{u} \quad (5)$$

$$\frac{w}{L}=\frac{gm1^2}{uncox\ \ Id5}=\frac{W1}{L1}=\frac{W2}{L2}=\frac{94.25^2}{110\ \times\ 30}\approx\frac{540n}{180n}$$

Step 5 design size of m5 noms transistor

$$Vds\ sat5=Vin(min)-Vss-\sqrt[2]{\frac{I5}{B_1}}-\mathrm{th1}\,max=-1+2.5-\sqrt[2]{\frac{30}{110\ \times3}}-0.85=0.35\,v$$

$$\frac{W5}{L5}=\frac{2\times Id5}{Un\times Vds\ sat5}=\frac{2\ \times30}{110\ (0.35)^2}=\frac{810n}{180n}$$

Step 6 design size of m6 pmos transistor

$$\mathrm{gm6}\geq10\ \times\mathrm{gm1}=942.5\ \mathrm{u}$$

$$\mathrm{gm4}=\sqrt[2]{Id5\ \times upcox\ \frac{W4}{L4}}=\mathrm{gm4}=\sqrt[2]{30\times50\times15}=150u$$

$$\frac{W6}{L6}=\frac{gm6}{gm4}\times\frac{W4}{L4}=\frac{W6}{L6}=\frac{942.5u}{150u}\times\frac{2700n}{180n}\approx\frac{17000n}{180n}$$

Step 7 design m7 noms transistor

$$\frac{W7}{L7}=\frac{I6}{I5}\times\frac{W5}{L5}\approx\frac{16500N}{180n}$$

4.2 THE OP-AMP DESGIN WAS BUILT IN TWO STAGE WITH THE FOLLOWING SPECIFICATION:

Table I provides a overview of the two-stage op amp design goals for this discussion. and the values were selected based on their viability and practicality for biomedical applications. Choosing a constant VDD value of 2.5 V allowed for ultra-low power operation. Equation [7] displays the design constant from Table 2 data. Table 3: Evaluation of Related Works The CMOS operational amplifier's transient analysis at 180 nm is shown in Fig. 4, and the phase margin is shown in Figure. 5.

Table 1. - Design goal

gain	Unity gain bandwidth	Maximum power disputation	Phase margin	Slew rate
60 dB	10MHz	2m wat	60.878532°	10 v/u se

Table 2. - constant design transistor

	vth	U	Lamda
PMOS	-0.7	50	0.05
NMOS	0.7	110	0.04

Table 3. - comparison with other work

	ICMR-	ICMR+	Slew rate	Gain bandwidth	Phase margin in degree	Cc	Bias current	Power supply	Technology channel nm
Paper design	0.8	1.8	20	10	60	15	30u	2.5	180 nm
[9]	-	-	-	40	89	-	-	3.5	180 nm
[10]	0.8	1.6	-	668	60	100	160	1.8	180 nm
[11]	-	-	2.34	0.37	-	-	-	1.8	180 nm

Each MOSFET's W/L values were calculated using equation [4], and the drain current was calculated using the Vdd value and the maximum permitted power dissipation. After doing a DC analysis on the first stage of the op amp and accurately determining the aspect ratios of all MOSFETs, the DC bias of VREF1 was altered based on gain considerations. The gain for the full amplifier was then corrected by adjusting VREF2.

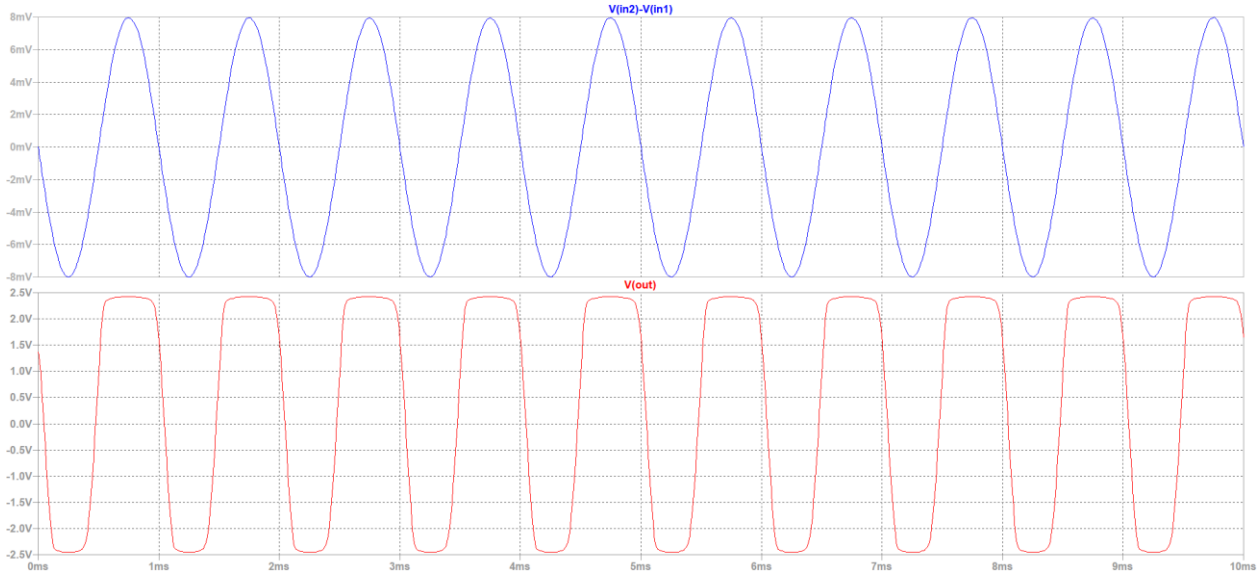

FIGURE 4. - the transient analysis of the CMOS operational amplifier at 180 nm

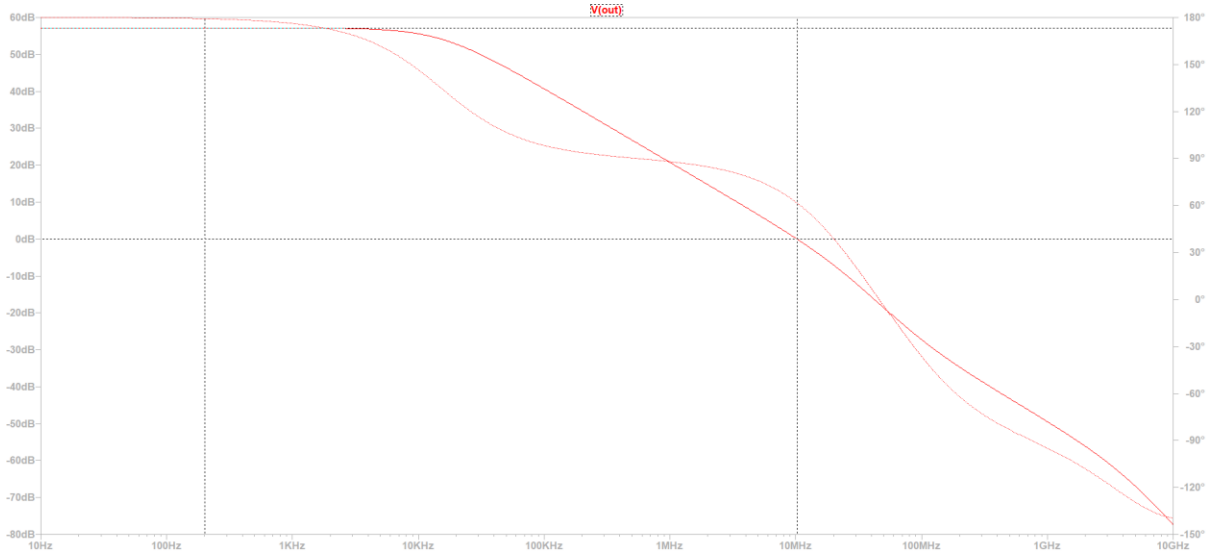

FIGURE 5. - the phase margin at 180 nm.

5. CONCLUSION

The two-stage op-amp design strategy was presented in this article. Scaling of device parameters formed the basis of this strategy. The amount of power dissipation met the 2 mW standards. The op-amps' operating range was determined by their IV characteristic. All of the transistors in this design were operated in the saturation region. Around 0.7 V, the transistor began to function at the saturation area. To assess an op-stability, amp's AC analysis was utilized. Because the compensation capacitor might impair the op-stability, amp's it was included. The resulting gain margin and phase margin were respectively 30 dB and 91.82°.

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CONFLICTS OF INTEREST

The authors declare no conflict of interest

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